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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Simon Robert Walmsley

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SILVERBROOK RESEARCH PTY LTD
393 DARLING STREET
BALMAIN, 2041
AUSTRALIA

EXAMINER

TRUVAN, LEYNNA THANH

ART UNIT

PAPER NUMBER

2435

MAIL DATE

DELIVERY MODE

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/727,180	Applicant(s) WALMSLEY ET AL.	
	Examiner Leynna T. Truvan	Art Unit 2435	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 June 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-3 are pending.

Response to Arguments

2. Applicant's arguments filed 6/25/2008 have been fully considered but they are not persuasive.

Examiner would like to thank applicant's representative for understanding that Bergum was applied to the claimed invention. For the record, Examiner would like to note that the correct US patent number of Bergum was used, only the name was inadvertent mentioned. Claims 1-3 remains rejected in view of Gilbert, et al. and Bergum, et al.

Examiner traverses the argument that Bergum does not teach or suggest operation of the keyed devices can be obscured by arranging the tamper circuitry directly over each bit of the keyed devices. Gilbert suggests passing directly over each bit of the non-volatile memory which broadly suggests scanning through or looking over the memory contents (bits) in order to detect tamper (Gilbert - col.6, lines 17-65). Bergum is brought forth to disclose the tamper detection line to obscure operation. Bergum provide a tamper loop and tamper detect circuit where the tamper loop is an electrical path that must be broken in order to physically access any device containing key information that is for greater security in storing and utilizing encryption/decryption keys in a non-volatile memory where the placement of keys in the EEPROM inherently

causes risks (Bergum-col.3, line 63 – col.4, line 7). Thus, would have been obvious for a person of ordinary skills in the art with tamper detection line of Bergum to pass directly over each bit of the non-volatile memory of Gilbert (Gilbert - col.6, lines 17-65 and col.7, lines 43-45) so as to obscure operation of the non-volatile memory of Bergum because this provide maximum key security the communication unit much be protected against tampering by an adversary (Bergum – col.3, line 63 – col.4, line 7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilbert, et al. (US 7,165,177), and further in view of Bergum, et al. (US 5,457,748).

As per claim 1:

Gilbert discloses a plurality of integrated circuits, each of the integrated circuits (col.1, lines 13-14 and col.4, lines 14-15) comprising a processor and non-volatile memory (col.5, lines 39-40 and col.7, lines 41-53) [and a tamper detection line

*arranged to pass directly over each bit of the non-volatile memory (col.6, lines 17-65 and col.7, lines 43-45) so as to obscure operation of the non-volatile memory] pass directly over each bit of the non-volatile memory, and including code for running identical software processes, wherein each of the integrated circuits also includes secret information used by the software process (col.2, lines 4-10 and col.6, lines 11-14; **secret information can broadly interpret as data that is protected and secure such that may involve authentication or verification process. Gilbert's secret key, authentication data, or certificate value (col.3, lines 1-28) which is referring to the claimed secret information.**), the secret information in each chip being located in a different location in the memory relative to a plurality of the other chips. (col.6, lines 18-22 and col.7, lines 55-65)*

Although, Gilbert discloses the invention that provides hardwired logic or microprocessor integrated circuit chips with protection against fraud (col.1, lines 10-15). Gilbert discusses passing directly over each bit of the non-volatile memory by the number of bits determines to prevent any attempt at fraudulent replaying and the number of m is the same as the number of bits in the certificate S where the masked certificate S does not reveal any information on the certificate (col.6, lines 18-67 and col.7, lines 1-25). Thus, obviously suggests the passing directly over each bit of non-volatile memory so as to obscure operation of the non-volatile memory. However, Gilbert did not go into details of a tamper detection line arranged to pass directly over each bit of the non-volatile memory so as to obscure operation of the non-volatile memory.

Bergum discloses an invention that provides a method and apparatus for greater security in storing and utilizing encryption/decryption keys in a non-volatile memory such as EEPROM (col.2, lines 32-38). There includes a microcontroller, encryptor, and decryptor that may comprise either a single or separate IC devices (col.2, lines 60-63). Bergum discloses the placement of keys in the EEPROM inherently causes risks, thus to provide maximum key security the communication unit must be protected against tampering by an adversary. This is accomplished with a tamper loop and tamper detect circuit where the tamper loop is an electrical path that must be broken in order to physically access any device containing key information. If an attempt is made to disassemble or tamper with the communication unit, the tamper circuit will trigger the microcontroller to erase the key stored in the decryptor (col.3, line 63 – col.4, line 7).

Therefore, it would have been obvious for a person of ordinary skills in the art to at the time the invention was made to include a tamper detection line arranged to obscure operation of the non-volatile memory to the integrated circuit chips of Gilbert in view of the teachings of Bergum because provide maximum key security the communication unit much be protected against tampering by an adversary (Bergum – col.3, line 63 – col.4, line 7).

As per claim 2: see Gilbert on col.6, lines 18-22 and col.7, lines 55-65; discussing a plurality of integrated circuits according to claim 1, wherein the code on each integrated

circuit is such that the software process of each chip knows the location in memory via which the secret information is accessible.

As per claim 3: Gilbert discusses a method of manufacturing a plurality of the integrated circuits of claim 2, including the steps of: manufacturing a plurality of physical integrated circuits; and **(col.5, lines 21-23)** injecting, into the non-volatile memory of each of the integrated circuits: code for running a software process; and secret information; **(col.4, lines 4-15 and col.6, lines 24-26)** wherein the secret information is positioned in relatively different locations of the non-volatile memories and the code on each integrated circuit is such that the software process of each integrated circuit knows the location in memory via which the secret information is accessible on that integrated circuit. **(col.6, lines 18-22 and col.7, lines 55-65)**

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leynna T. Truvan whose telephone number is (571) 272-3851. The examiner can normally be reached on Monday - Thursday (7:00 - 5:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on (571) 272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/L. T. T./
Examiner, Art Unit 2435
/KimYen Vu/
Supervisory Patent Examiner, Art Unit 2435